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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/606,463	06/26/2003	Benjamin Thomas Percer	200208051-1	3495
22879	7590	12/13/2004		
HEWLETT PACKARD COMPANY P O BOX 272400, 3404 E. HARMONY ROAD INTELLECTUAL PROPERTY ADMINISTRATION FORT COLLINS, CO 80527-2400				EXAMINER BHAT, ADITYA S
				ART UNIT 2863 PAPER NUMBER

DATE MAILED: 12/13/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/606,463	PERCER ET AL.	
	Examiner	Art Unit	
	Aditya S Bhat	2863	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --
Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

- 1) Responsive to communication(s) filed on 26 June 2003.
 2a) This action is FINAL. 2b) This action is non-final.
 3) Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

- 4) Claim(s) 1-22 is/are pending in the application.
 4a) Of the above claim(s) _____ is/are withdrawn from consideration.
 5) Claim(s) _____ is/are allowed.
 6) Claim(s) 1-5,8,10-14 and 16-22 is/are rejected.
 7) Claim(s) 6,7,9 and 15 is/are objected to.
 8) Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

- 9) The specification is objected to by the Examiner.
 10) The drawing(s) filed on 26 June 2003 is/are: a) accepted or b) objected to by the Examiner.
 Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).
 Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).
 11) The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

- 12) Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
 a) All b) Some * c) None of:
 1. Certified copies of the priority documents have been received.
 2. Certified copies of the priority documents have been received in Application No. _____.
 3. Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

- | | |
|--|---|
| 1) <input checked="" type="checkbox"/> Notice of References Cited (PTO-892) | 4) <input type="checkbox"/> Interview Summary (PTO-413) |
| 2) <input type="checkbox"/> Notice of Draftsperson's Patent Drawing Review (PTO-948) | Paper No(s)/Mail Date. _____ |
| 3) <input checked="" type="checkbox"/> Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08)
Paper No(s)/Mail Date <u>6/26/03</u> . | 5) <input type="checkbox"/> Notice of Informal Patent Application (PTO-152) |
| | 6) <input type="checkbox"/> Other: _____ |

DETAILED ACTION

Claim Rejections - 35 USC § 102

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless –

(b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

Claims 1-5, 8, 10-14 and 16-22 rejected under 35 U.S.C. 102(b) as being anticipated by Co et al. (USPN 6,351,827).

With regards to claim 1, Co et al. (USPN 6,351,827) teaches a system for voltage margin testing of one or more components of said system, comprising:

a controller internal to said electronic system; (Col. 6, lines 13-15) and
a digital voltage adjuster in communication with said controller and with said one or more components, said voltage adjuster affecting generation of one or more test voltages for application to said components in response to commands from the controller. (Col. 6, lines 22-24)

With regards to claim 2, Co et al. (USPN 6,351,827) teaches a diagnostics software executing to collect and analyze data regarding a response of said system to said test voltages. (Col. 6, lines 11-12 & 36-37)

With regards to claim 3, Co et al. (USPN 6,351,827) teaches a power rail electrically coupled to said components for applying voltage thereto, said voltage adjuster being electrically coupled to said power rail to set said power rail voltage to one or more of said test voltages. (38;figure 2)

With regards to claim 4 and 17, Co et al. (USPN 6,351,827) teaches a voltage regulator receiving an input voltage and generating a regulated output voltage for application to said power rail, said voltage adjuster being coupled to said regulator for varying said regulated output voltage in response to commands from said controller. (Col. 6,lines 32-33)

With regards to claim 5 and 18, Co et al. (USPN 6,351,827) teaches a digital potentiometer incorporated in a feedback circuitry of said voltage regulator, wherein the digital potentiometer varies a resistance associated with said feedback circuitry in response to commands from said controller so as to vary said output voltage of the regulator. (Col. 6, lines 22-24)

With regards to claim 8 and 20, Co et al. (USPN 6,351,827) teaches controller is a Baseboard Management Controller (BMC). (Col.5, line 54)

With regards to claim 10, 16 and 21 Co et al. (USPN 6,351,827) teaches I²C based bus for providing communication between said BMC and said voltage adjuster.(Col.8, lines 36-46)

With regards to claim 11, Co et al. (USPN 6,351,827) teaches said controller initiates margin testing in response to a command from an external system. (Col.8, lines 37-39)

With regards to claim 12 and 13, Co et al. (USPN 6,351,827) teaches a computer system that is a server. (Col.2, lines 29-30)

With regards to claim 14, Co et al. (USPN 6,351,827) teaches a computer system, comprising:

a processor; (Col. 6, lines13-15)

a plurality of components in communication with said processor for performing a plurality of tasks; (Col. 6, lines13-15)

a controller; (Col. 6, lines13-15) and

a digital voltage adjuster in communication with said controller and one or more of said components, said adjuster affecting generation of one or more test voltages for application to selected ones of said components for voltage margin testing thereof in response to commands from said controller. (Col. 6, lines 22-24)

With regards to claim 19, Co et al. (USPN 6,351,827) teaches a method for voltage margin testing of one or more components of an electronic system, having an internal controller, and a digital voltage adjuster, in communication with said controller and with at least a power rail supplying voltage to said components, comprising:

causing the controller to transmit one or more commands to said voltage adjuster to cause the adjuster to affect generation of one or more test voltages at said power rail for application to said components, (Col. 6, lines15-24) and

monitoring response of said computer system to each of said test voltages. (Col. 8, lines 59-67)

With regards to claim 22, Co et al. (USPN 6,351,827) teaches utilizing a hardware monitor to measure voltage at said power rail and transmitting said measured voltage to said controller. (Col. 8, lines 37-45)

Allowable Subject Matter

The following is a statement of reasons for the indication of allowable subject matter: Claims 6-7,9 &15 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

Conclusion

The prior art made of record and not relied upon is considered pertinent to applicant's disclosure. King (USPN 6,697,952) teaches a margin processor power supply.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Aditya S Bhat whose telephone number is 571-272-2270. The examiner can normally be reached on M-F 9-5:30.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, John Barlow can be reached on 571-272-2269. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see <http://pair-direct.uspto.gov>. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

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Aditya S Bhat
December 8, 2004



John Barlow
Supervisory Patent Examiner
Technology Center 2800